SGS-THOMSON MICROELECTRONICS

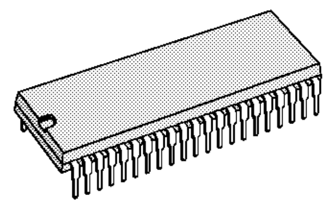
TEA5040S

WIDE BAND VIDEO PROCESSOR

- DIGITAL CONTROL OF BRIGHTNESS, SATURATION AND CONTRAST ON TV SIGNALS AND R, G, B INTERNAL OR EXTERNAL SOURCES
- BUS DRIVE OF SWITCHING FUNCTIONS
- DEMATRIXING OF R, G, B SIGNALS FROM Y, R-Y, B-Y, TV MODE INPUTS
- MATRIXING OF R, G, B SOURCES INTO Y, R-Y, B-Y SIGNALS
- AUTOMATIC DRIVE AND CUT-OFF CONTROLS BY DIGITAL PROCESSING DURING FRAME RETRACE
- PEAK AND AVERAGE BEAM CURRENT LIMITATION
- ON-CHIP SWITCHING FOR R, G, B INPUT SELECTION
- ON-CHIP INSERTION OF INTERNAL OR EXTERNAL R, G, B SOURCES

DESCRIPTION

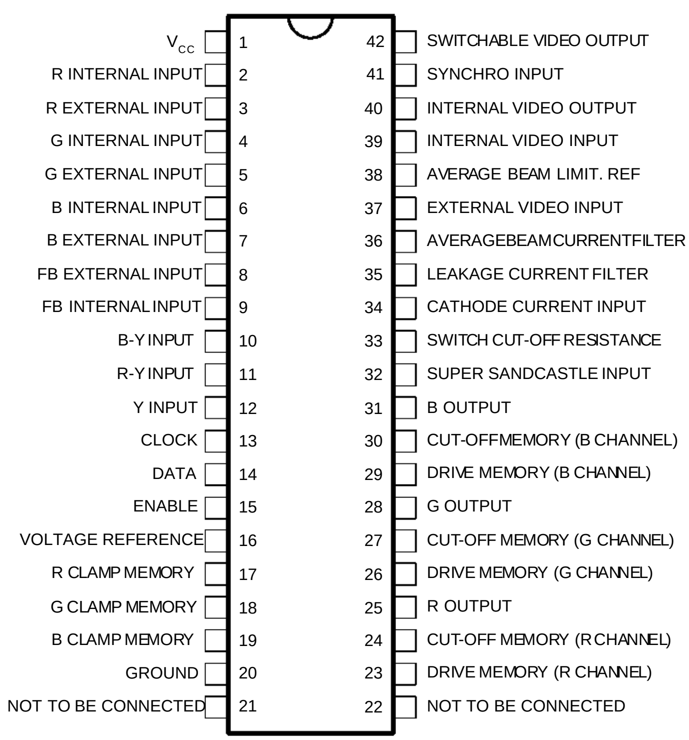
The TEA5040S is a serial bus-controlled video-processing device which integrates a complex architecture fulfilling multiple functions.



SDIP42
(Plastic Package)

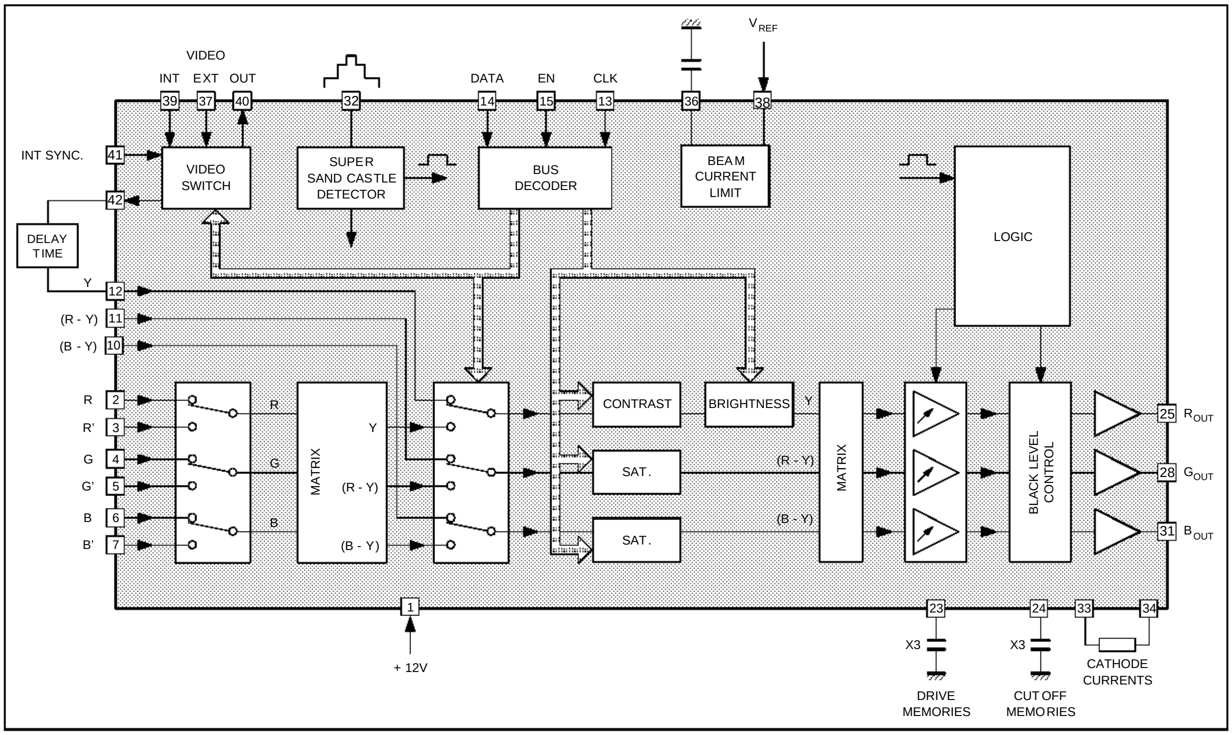
ORDER CODE : TEA5040S

PIN CONNECTIONS



5040S-01.EPS

BLOCK DIAGRAM



GENERAL DESCRIPTION

Brief Description

This integrated circuit incorporates the following features :

- a synchro and two video inputs
- a fixed video output
- a switchable video output
- normal Y, R-Y, B-Y TV mode inputs
- double set of R, G, B inputs
- brightness, contrast and saturation controls as well on a R, G, B picture as on a normal TV picture
- digital control inputs by means of serial bus
- peak beam current limitation
- average beam current limitation
- automatic drive and cut-off controls

Block Diagram Description

BUS DECODER

A 3 lines bus (clock, data, enable) delivered by the microcontroller of the TV-set enters the videoprocessor integrated circuit (pins 13-14-15). A control system acts in such a way that only a 9-bit word is taken into account by the videoprocessor. Six of the bits carry the data, the remaining three carry the address of the subsystem.

Function	Address	Number of Bits
Brightness Control	0	5
Contrast Control	1	5
Colour on/off Selection	2	1
Insertion Allowed	3	1
Sync/Async Mode	4	1
Int/Ext Video Switching	5	1
B-Y Saturation Control	6	6
R-Y Saturation Control	7	6

Table below depicts 9-bit words required for various functions.

Subsystem's Configuration		Data Bits LSB....MSB	Add. Bits LSB....MSB
BRIGHTNESS	Min. Max.	X00000 X11111	000
CONTRAST	Min. max.	X00000 X11111	100
COLOUR ON/OFF	Off On	XXXXX0 XXXXX1	010
INSERTION	Allowed Not Allow.	XXXXX0 XXXXX1	110
SYNC/ASYNC MODE	Sync. Async.	XXXX0X XXXX1X	001
VIDEO INT/EXT	Ext. Int.	XXXXX0 XXXXX1	101
SATURATION B-Y	Min. Max.	000000 111111	011
SATURATION R-Y	Min. Max.	000000 1111	111

A demultiplexer directs the data towards latches which drive the appropriate control. More detailed information about serial bus operation is given in the following chapter.

Video Switch

The video switch has three inputs :

- an internal video input (pin 39),
- an external video input (pin 37),
- a synchro input (pin 41),

and two outputs :

- an internal video output (pin 40),
- a switchable video output (pin 42)

The 1Vpp composite video signal applied to the internal video input is multiplied by two and then appears as a 2Vpp low impedance composite video signal at the output. This signal is used to deliver a 1Vpp/75Ω composite video signal to the peri-TV plug.

The switchable video output can be any of the three inputs. When the Int/Ext one active bit word is high (address number 5), the internal video input is selected. If not, either a regenerated synchro pulse or the external video signal is directed towards this output depending on the level of the Sync/Async one active bit word (address number 4). As this output is to be connected to the synchro integrated circuit, RGB information derived from an external source via the Peri-TV plug can be displayed on the screen, the synchronization of the TV-set being then made with an external video signal.

When RGB information is derived from a source integrated in the TV-set, a teletext decoder for example, the synchronization can be made either on the internal video input (in case of synchronous data) or on the synchro input (in case of asynchronous data).

R, G, B Inputs

There are two sets of R, G, B inputs : one is to be connected to the peri-TV plug (Ext R, G, B), the second one to receive the information derived from the TV-set itself (Int R, G, B).

In order to have a saturation control on a picture coming from the R, G, B inputs too, it is necessary to get R-Y, B-Y and Y signals from R, G, B information : this is performed on the first matrix that receives the three 0.9Vp (100% white) R, G, B signals and delivers the corresponding Y, R-Y, B-Y signals. These ones are multiplied by 1.4 in order to make the R-Y and B-Y signals compatible with the R-Y and B-Y TV mode inputs. The desired R, G, B inputs are selected by means of 3 switches controlled by the two fast blanking signal inputs. A high level on FB external pin selects the external RGB sources. The three selected inputs are clamped in order to give the required DC level at the output of this first matrix. The three not selected inputs are clamped on a fixed DC level.

Y, R-Y, B-Y Inputs

The 2Vpp composite video signal appearing at the switchable output of the video switch (pin 42) is driven through the subcarrier trap and the luminance delay line with a 6 dB attenuation to the Y input (1Vpp ; pin 12). In order to make this 1Vpp (synchro to white) Y signal compatible with the 1Vpp (black to white) Y signal delivered by the first matrix, it is necessary to multiply it by a coefficient of 1.4.

R, G, B Insertion Pulse (fast blanking)

A R, G, B source has also to provide an insertion

pulse. Since this integrated circuit can be directly connected to two different sources, it is necessary then to have two separate insertion pulse inputs (pin 8-9). Fast blanking can be inhibited by a one active bit word. The two fast blanking inputs carry out an OR function to insert R, G, B sources into TV picture. The external fast blanking (FB ext.) selects the appropriate R, G, B source.

Controls

The four brightness, contrast and saturation control functions are direct digitally controlled without using digital-to-analog converters.

The contrast control of the Y channel is obtained by means of a digital potentiometer which is an attenuator including several switchable cells directly controlled by a 5 active bit word (address number 1). The brightness control is also made by a digital potentiometer (5 active bit word, address number 0). Since a + 3dB contrast capability is required, the Y signal value could be up to 0.7Vpp nominal. For both functions, the control characteristics are quasi-linear.

In each R-Y and B-Y channel, a six-cell digital attenuator is directly controlled by a 6 active bit word (address number 6 and 7). The tracking needed to keep the saturation constant when changing the contrast has to be done externally by the microcontroller. Furthermore, colour can be disabled by blanking R-Y and B-Y signals using one active bit word (address number 2) to drive the one-chip colour ON/OFF switch.

Second Matrix, Clamp, Peak Clipping, Blanking

The second matrix receives the Y, R-Y and B-Y signals and delivers the corresponding R, G, B signals. As it is required to have the capability of + 6dB saturation, an internal gain of 2 is applied on both R-Y and B-Y signals.

A low clipping level is included in order to ensure a correct blanking during the line and frame retraces. A high clipping level ensures the peak beam current limitation. These limitations are correct only if the DC bias of the three R, G, B signals are precise enough. Therefore a clamp has been added in each channel in order to compensate for the inaccuracy of the matrix.

Sandcastle Detector And Counter

The three level supersandcastle is used in the circuit to deliver the burst pulse (CLP), the horizontal pulse (HP), and the composite vertical and horizontal blanking pulse (BLI). This last one is regenerated in the counter which delivers a new composite pulse (BL) in which the vertical part lasts 23 lines when the vertical part of the supersandcastle lasts more than 11 lines.

The TEA5040S cannot work properly if this minimum duration of 11 lines is not ensured.

The counter delivers different pulses needed circuit and especially the line pulses 17 to 23 used in the automatic drive and cut-off control system.

Automatic Drive And Cut-off Control System

Cut-off and drive adjustments are no longer required with this integrated circuit as it has a sample and hold feedback loop incorporating the final stages of the TV-set. This system works in a sequential mode. For this purpose, special pulses are inserted in G, R and B channels. During the lines 17, 18 and 19, a ”drive pulse” is inserted respectively in the green, red and blue channels. The line 20 is blanked on the three channels. During the lines 21, 22 and 23, a ”quasi cut-off pulse” is inserted respectively in the green, red and blue guns.

The resulting signal is then applied to the input of a voltage controlled amplifier. In the final stages of the TV-set, the current flowing in each green, red and blue cathode is measured and sent to the videoprocessor by a current source.

The three currents are added together in a resistor matrix which can be programmed to set the ratio between the three currents in order to get the appropriate colour temperature. The output of the matrix forms a high impedance voltage source which is connected to the integrated circuit (pin 34). Same measurement range between drive and cut-off is achieved by internally grounding an external low impedance resistor during lines 17, 18 and 19.

This is due to the fact that the drive currents are about one hundred times higher than the cut-off and leakage currents.

Each voltage appearing sequentially on the wire pin 34 is then a function of specific cathode current :

- When a current due to a drive pulse occurs, the voltage appearing on the pin 34 is compared within the IC with an internal reference, and the result of the comparison charges or discharges an external appropriate drive capacitor which stores the value during the frame. This voltage is applied to a voltage controlled amplifier and the system works in such a way that the pulse current drive derived from the cathode is kept constant.
- During the line 20, the three guns of the picture tube are blanked. The leakage current flowing out of the final stages is transformed into a voltage

which is stored by an external leakage capacitor to be used later as a reference for the cut-off current measurement.
- When a current due to a cut-off pulse occurs, the voltage appearing on the pin 34 is compared within the IC to the voltage present on the leakage memory. An appropriate external capacitor is then charged or discharged in such a way that the difference between each measured current and the leakage current is kept constant, and thus the quasi cut-off current is kept constant.

Average Beam Current Limitation

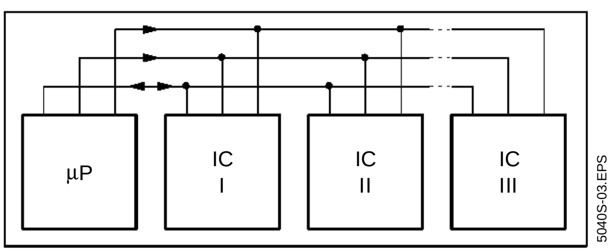
The total current of the three guns is integrated by means of an internal resistor and an external capacitor (pin 36) and then compared with a programmable voltage reference (pin 38). When 70% of the maximum permitted beam current is reached, the drive gain begins to be reduced ; to do so, the amplitude of the inserted pulse is increased.

In order to keep enough contrast, the maximum drive reduction is limited to 6dB. If it is not sufficient, the brightness is suppressed.

SPECIFICATION FOR THE THOMSON BI-DIRECTIONAL DATA BUS

This is a bi-directional 3-wire (ENABLE, CLOCK, DATA) serial bus. The DATA line transmission is bi-directional whereas ENABLE and CLOCK lines are only microprocessor controlled. The ENABLE and CLOCK lines are only driven by the microcomputer.

Figure 1



It is possible to select several IC from the microprocessor via the bus. The identification of each particular IC is achieved by the length of the word (number of data bits/clock pulses), meaning that each IC responds with its own particular word length.

The number is determined while ENABLE is low and by counting the negative clock edges. As soon as the high edge of the ENABLE signal is applied, the number is fixed (see Figure 2).
The reply word lenght from any of the IC on the bi-directional line is four bits. If it is found insufficient then the reply word can be expanded to include two repetitive reply sequences one after the other.

The bi-directional transmission is enabled if :
- the IC has been previously addressed at the positive going edge of the enable pulse.
- ENABLE remains high,
  and DATA is available only during the period when the clock remains low.
- number of identification bits : n
  1...n : data from the microcomputer
- number of bi-directional clocks : 4
  1...M : data to the microcomputer

The four bit reply word (synchronized with the clock coming from the microcontroller) from the addressed IC to the microcontroller is sent only once. Subsequent clock pulses present on the clock line will be ignored by the IC in question. The data sent to the microcontroller can generally be suppressed completely or partially, but in the case of the videoprocessor, a minimum reply word lenght of 1 has to be maintained (see Figure 3).

This implies that a bi-directional bus that incorporates other IC's together with a videoprocessor IC is then also limited by the minimum reply word restriction of 1.

The data word from the microcompter is divided into :
- addresses within the IC
- data

The data word to the microcomputer is divided into
- two data bits,
- two address bits

After the operating voltage is applied, the first transmission will be used as a reset command, i.e. the data word will not be detected.
- number of identification bits : n
  1...n : data from the microcomputer
- number of bi-directional clocks : 1
  1 : data the microcomputer (which is the minimum number for the videoprocessor)

Figure 2

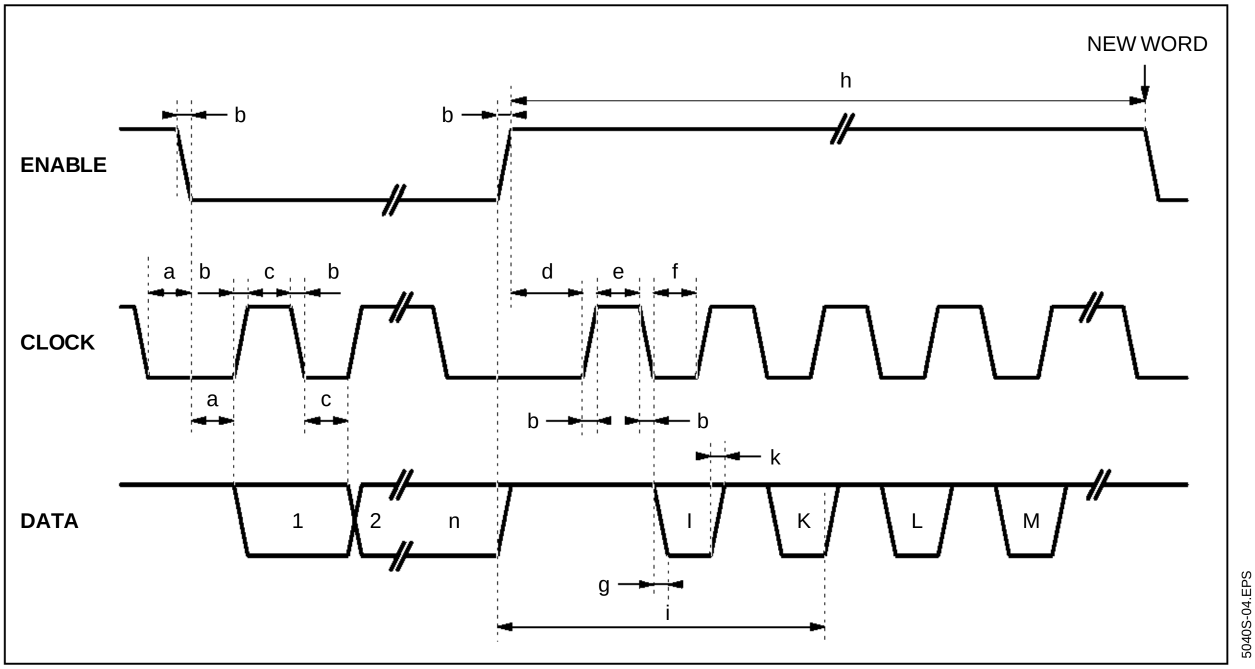
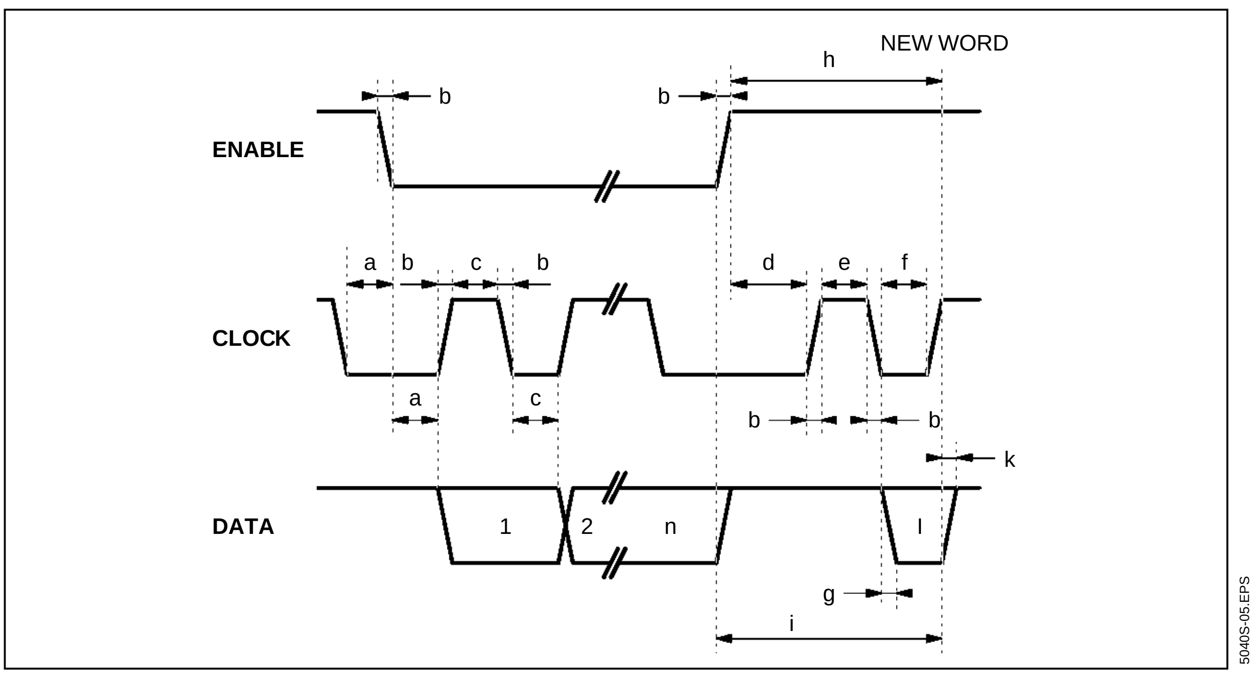


Figure 3



BI-DIRECTIONAL DATA BUS

Symbol	Parameter	Min.	Typ.	Max.	Unit
TIMING Identification nr-9 (9 video processor address) (see figures 2-3)					
a		5			µs
b		0			µs
c		5			µs
d		70			µs
e	N/A				
f	N/A				
g	N/A				
h	new word to same IC new word to other IC	24 70			ms µs

5040S-01.TBL

ABSOLUTE MAXIMUM RATINGS

T_{AMB} = 25°C (unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Pin 1	14			V
T_{OPER}	Operating Temperature Range	0, + 60			°C
T_{STG}	Storage Temperature Range	– 25, + 125			°C

5040S-02.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th(j-a)}$	Junction-ambiant Thermal Resistance	Typ.	60	°C/W

5040S-03.TBL

ELECTRICAL OPERATING CHARACTERISTICS (T_{AMB} = 25°C, V_{CC} = 12V, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Pin 1	10.8	12	12.5	V
I_{CC}	Supply Current Pin 1		80	104	mA
VIDEO SWITCH					
	External Video Input (75Ω source impedance)				
V_{37}	Signal Amplitude Pin 37		1	1.4	Vpp
I_{37}	Input Current Pin 37		10	30	µA
	Internal Video Input (300Ω source impedance)				
V_{39}	Signal Amplitude Pin 39		1	1.4	Vpp
I_{39}	Input Current Pin 39		10	30	µA
	Synchro Input				
	Output Signal Amplitude Pin 42 (for a 0.5V input signal on pin 41)	0.5	0.6		V
	Internal Video Output Pin 40				
	Dynamic	2.7			Vpp
	DC Level (bottom of synchro pulse)	1		2	V
	Gain between Pin 39 (for 1Vpp on pin 39) and Pin 40	5	6	7	dB
	Crosstalk between Pin 37 and Pin 40)			– 50	dB
	Bandwidth (– 1dB)	6			MHz
	Switchable Video Output Pin 42				
	Dynamic (pin 37 or pin 39 selected)	2.7			Vpp
	Gain between Pins 37 and 42 (for 1VPP on pin 37)	5		7	dB
	Gain between Pins 39 and 42 (for 1VPP on pin 39)	5			dB
	Crosstalk between Pins 37 or 39 with Pin 42			– 50	dB
	Bandwidth (– 1dB)			– 50	MHz

5040S-04.TBL

ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
TV MODE INPUTS					
	Luminance Input Pin 12				
Y	Signal Amplitude (100% white)		1	1.5	V_{pp}
V_{12}	DC Level (on black level)		4		V
I_{12}	Input Current			10	µA
	R-Y Input Pin 11				
R-Y	Signal Amplitude (75% saturation)		1.05	1.47	V_{pp}
V_{11}	DC Level (on black level)		4.7		V
I_{11}	Input Current			2	µA
	B-Y Input Pin 10				
B-Y	Signal Amplitude (75% saturation)		1.33	1.86	V_{pp}
V_{10}	DC Level (on black level)		4.7		V
I_{10}	Input Current			2	µA
RGB INPUTS PINS 2-3-4-5-6-7					
	Signal Amplitude (100% saturation without synchro pulse)		0.7	1	V_{pp}
	DC Level (on black level)		3.2		V
	Input Current			3	µA
FAST BLANKING INPUTS PINS 8-9					
	TV/RGB Mode Threshold	0.5		0.9	V
	Switching Time		70		ns
	Switching Time Delay		70		ns
CLAMP MEMORY OUTPUT PINS 17-18-19					
	Voltage Range	8	10	11	V
	Input Current			2	µA
REFERENCE PARAMETER					
V_{REF}	Reference Voltage Pin 16		4		V
SANDCASTLE INPUT PIN 32					
	Blanking Threshold	1	1.4	1.8	V
	Burst Gate Threshold	6.4	6.9	7.6	V
	Line Retrace Threshold	3.1	3.4	3.8	V
	Input Current Pin 32 Grounded			100	µA
DRIVE AND CUT-OFF MEMORY OUTPUT PINS 23-24-26-27-29-30					
	Drive Leakage Current Pins 23-26-29			1	µA
	Cut-off Leakage Current Pins 24-27-30			1	µA
	Minimum Active Level Pins 24-27-30		4		V
LEAKAGE CURRENT MEMORY OUTPUT PIN 35					
	Voltage Range	3			V
	Input Current (during picture pin 35 = 5V)			0.5	µA
	Charging Output Impedance			500	Ω
	Minimum Voltage (pin 34 grounded)		3		V
CATHODE CURRENTS INPUT PIN 34					
	Output Current during the Line Trace (pin 34 grounded)			10	µA
	Voltage during Lines 17, 18, 19	0.26	0.35	0.50	V
	Voltage Difference during Lines 21, 22, 23 and during Line 20		0.4		V

5040S-05.TBL

ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter		Min.	Typ.	Max.	Unit
CATHODE CURRENTS INPUT PIN 34 (continued)						
	Voltage Amplitude on Cathode Currents Input for Drive Decrease					
V_{34}	Threshold 10% on Drive/cut-off	1V on Pin 38 2V on Pin 38		0.7 1.4		V V
	Voltage Amplitude on Cathode Currents Input for Brightness					
V_{34}	Decrease Threshold	1V on Pin 38 2V on Pin 38		1 2		V V
IMPEDANCE SWITCH PIN 33)						
	Saturation Impedance [for 5mA] (open during lines 20, 21, 22, 23)			250		Ω
REFERENCE VOLTAGE INPUT FOR THE AVERAGE BEAM CURRENT LIMITER PIN 38						
V_{38}	Reference Voltage		0		5	V
I_{38}	Input Current (V_{38} = 1V)				– 20	V
AVERAGE BEAM CURRENT FILTER PIN 36 VOLTAGE RANGE						
	0 < V34 < 7V		6			V
RGB OUTPUTS R (PIN 25), G (PIN 28), B (PIN 31)						
	Inserted Levels					
	Low Clipping Level Referred to quasi Cut-off Inserted Level (100% = B/W output signal at maximum contrast with 0.5V (B/W) input Y signal)			45		%
	High Clipping Level Referred to quasi Cut-off Inserted Level (100% = B/W output signal at maximum contrast with 0.5V (B/W) input Y signal)			115		%
	Drive Inserted Level Referred to quasi Cut-off Inserted Level (without beam limitation, V_{38} = 6V, V_{34} grounded)			35		%
	Bandwidth (– 3dB) (TV mode and R, G, B mode)			10		MHz
	Crosstalk for any of the 11 Inputs Pins 2-3-4-5-6-7-10-11-12-37-39 on any of the 5 Outputs Pins 25-28-31-40-42 (range : DC to 1MHz)				– 50	dB
	Brightness					
	Nominal Brightness Referred to quasi Cut-off Inserted Level (bit word "10000" address = 0)			– 25		%
	Total Brightness Range (100 % = W/B output signal when 0.5V (W/B) on pin 12 and max. contrast)			78		%
	Maximum Brightness (100% = W/B output signal when 0.5V (W/B) on pin 12 and max. contrast)			38		%
	Minimum Brightness (100% = W/B output signal when 0.5V (W/B) on pin 12 and max. contrast)			– 40		%
	Differential Brightness between any two Channels (TV mode, colour off, pins 10-11-12 AC grounded, 0.5 (W/B) signal on Pin 12, maximum contrast = 100% on RGB outputs)			2		%
	Variation of the Differential Brightness (in the whole saturation control range (including colour off))			0.5		%
	Contrast : Max. Contrast Attenuation		11			dB
	Saturation					
	Max. Saturation			6		dB
	Max. Saturation Attenuation		20			dB
	Colour off Attenuation		40			dB

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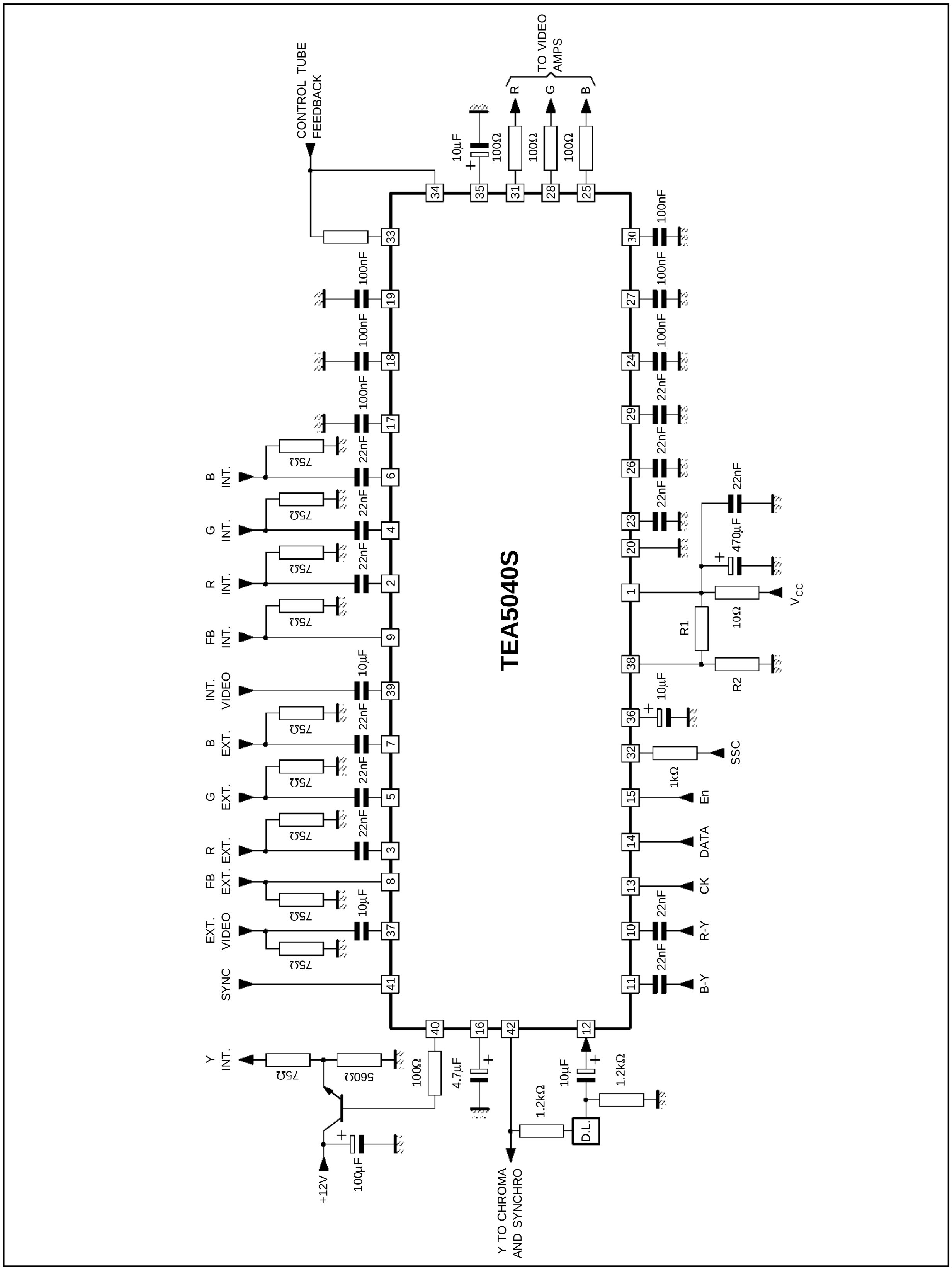
ELECTRICAL OPERATING CHARACTERISTICS (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
RGB OUTPUTS R (PIN 25), G (PIN 28), B (PIN 31) (continued)					
	Output Signal Amplitude Pins 25-28-31 (blanking to high clipping) • Y input : 0.7V B/W • 0dB Contrast, Bit Word = 010110, Address = 1 • Maximum Brightness • Maximum Drive Efficiency (Pins 23-26-29 grounded) • No Average Beam Current Limitation (Pin 38 to 6V)		6.2		V
	Black to White Output Voltage Y Input : 0.5V (B/W) Maximum Contrast (Pin 38 to 6V, Pins 23-26-29 grounded)		3.6		V
	Drive Efficiency Ratio : $\frac{V_{OUT} \text{ (Pins 23–26–29 grounded)}}{V_{OUT} \text{ (Pins 23–26–29 to } V_{CC})}$ (no average beam current limitation Pin 38 to 6V)		3.6		
	Black Level Control (variable DC voltage from 4V to V_{CC} on Pins 24-27-30)	4.3			V
BUS INPUTS PINS 13-14-15					
V_{HL}	High Level	3.5			V
V_{LL}	Low Level			1	V

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SGS-THOMSON MICROELECTRONICS

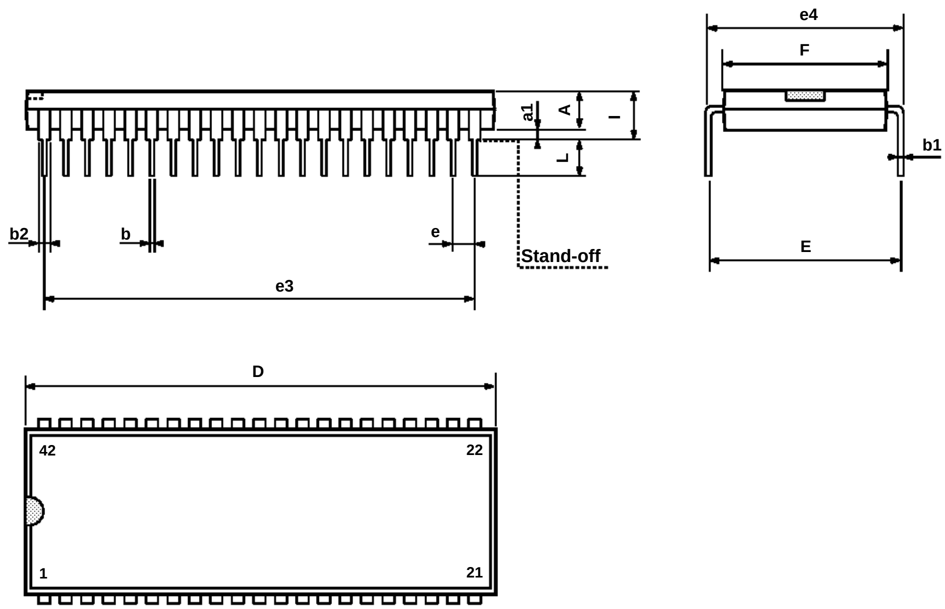
APPLICATION CIRCUIT



5040S-06.EPS

PACKAGE MECHANICAL DATA

42 PINS - PLASTIC SHRINK DIP



PMSDIP42.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.30			0.130		
a1		0.51			0.020	
b		0.35	0.59		0.014	0.023
b1		0.20	0.36		0.008	0.014
b2		0.75	1.42		0.030	0.056
b3		0.75			0.030	
D			39.12			1.540
E		15.57	17.35		0.613	0.683
e	1.778			0.070		
e3	35.56			1.400		
e4	15.24			0.600		
F			14.48			0.570
i			5.08			0.200
L		2.54			0.100	

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